HF preamps analysis with respect to BIAS sweep

It was found that the consumption peaks of the HF preamps are quite linked to the BIAS current sweeps.

A first analysis is proposed here, to understand the cause of these overconsumption peaks and the stress possibly caused on the HF preamps in normal operation. A second analysis aims to investigate the effects of the short-circuit failure on the integrity of the HF preamps.

Part 1: Behavior of HF preamps in normal operation

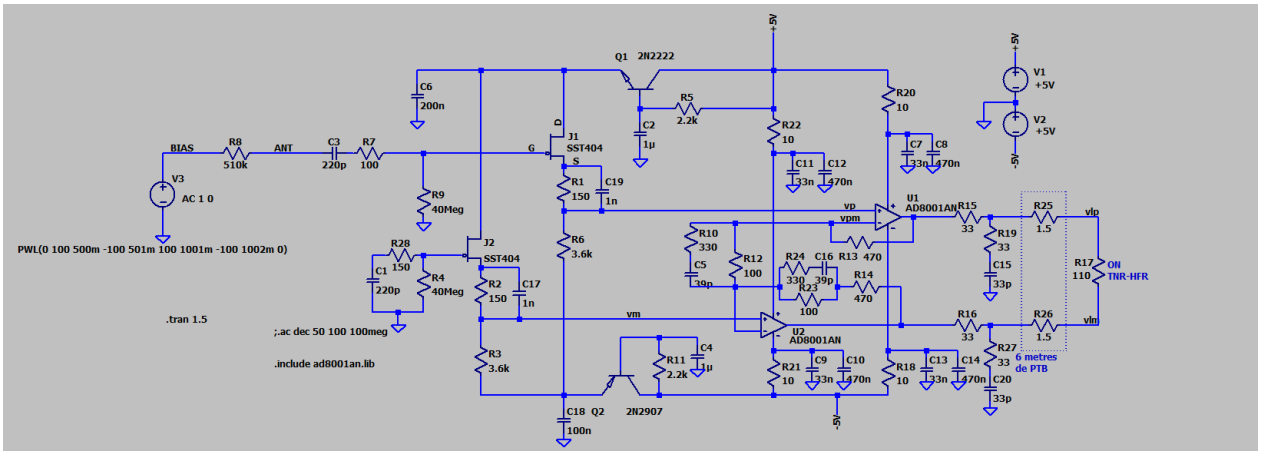
The assumptions made here are realistic in normal operation of RPW, but are not representative of the failure case encountered on ANT#3.

Simulation setup

The analysis is based on a complete model taking into account all stages of the preamp. The output impedance of the BIAS current source is also taken into account (set at 510 kohms).

At the HF preamp input, we apply a large ramp of +/-100V to simulate BIAS sweep using a sawtooth waveform. Additionally, the duration of the sweep is arbitrarily chosen to be much smaller than the actual duration of the sweep in flight. This further constrains the simulation results.

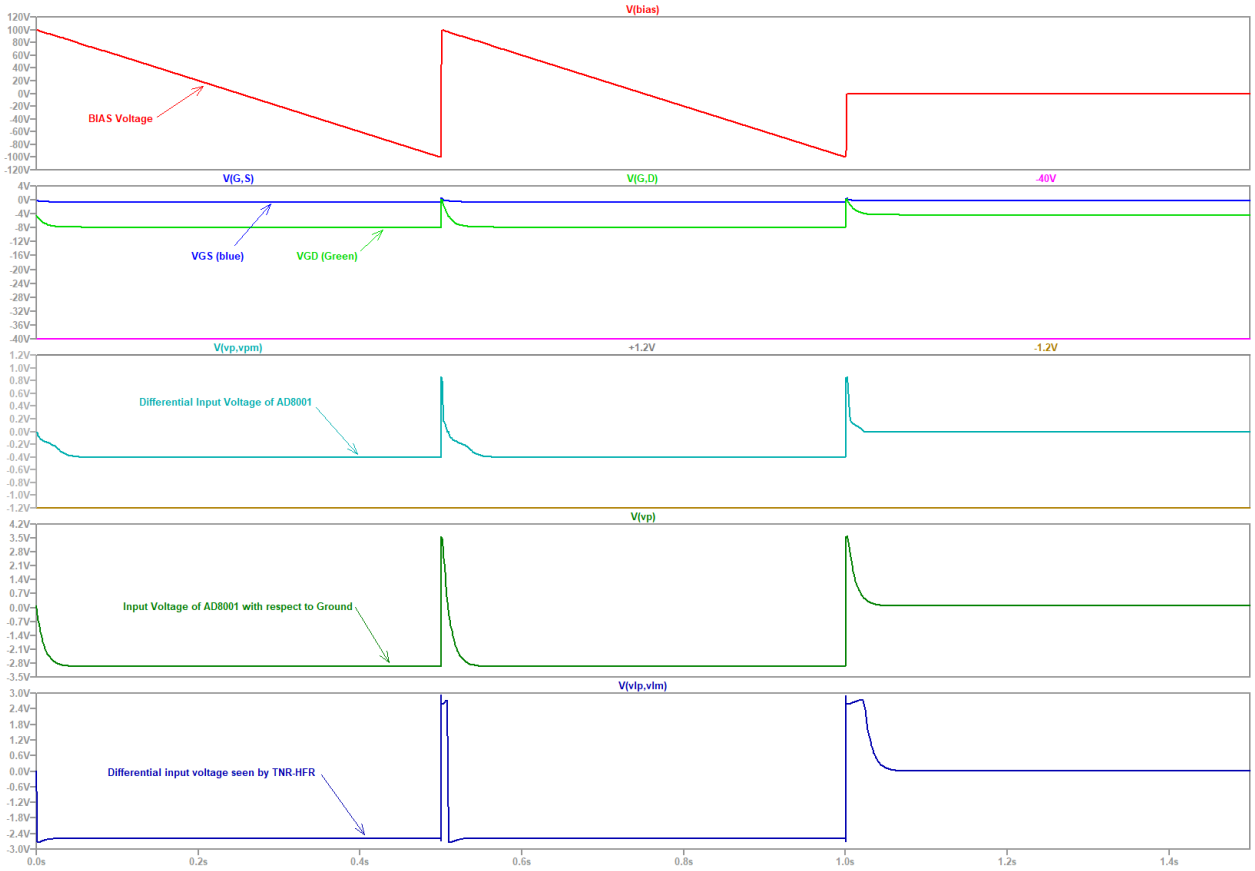
Transients caused by such a signal corresponds to an extreme worst case (the sweep used in flight is much more favorable).



Simulation results

The plots below give the responses of different intermediate signals from the HF preamp, namely:

- VGS, VGD at the JFET stage
- Differential signal at the input of the AD8001
- Ground referenced at the inputs of the AD8001
- Differential signal at the output of the preamp loaded by 110 ohms



What arises from these results?

1. The simulation shows that the derating constraints are meet with comfortable margins despite the large ramp of +/-100V
    - VGS is negligible and VGD < -8V; which is far below the -40V limit
    - Differential voltage is comprised between -0.4V and +0.8V, while the limit is +/-1.2V
2. In itself, this observation shows that there is no particular risk in having the BIAS sweep coexist with the HF preamp in operation. It might even be risky to turn it OFF under the pretext of protecting it from BIAS sweeps.
3. The waveform at the output of the preamps (differential signal in blue) shows a relatively narrow and intense pulse. This coincides with the rising edge of the BIAS sweep, which has the effect of saturating the HF preamp for a short duration. This voltage pulse results in excess consumption in the 110 ohms load, which explains the current peaks observed on the monitoring HKs.

This last conclusion, however, has no harmful consequences on HF preamps. After saturation recovery, the HF preamp resumes normal operation without any particular stress.

One possible option to mitigate the problem (which is not necessarily a problem) would be to “smooth” the BIAS sweep : i.e. sweep consisting of an ascending ramp followed by a descending ramp.

About possible latch-up

A latch-up in an electronic circuit is characterized by a persistent state, which causes overconsumption (observable on the power rails). When it occurs, it usually does not go away on its own. To release it requires an on/off cycle.

This aspect has been carefully taken into account during the design and the latch-up immunity was verified by applying +/-100V short transients to the preamp input. Latch-up never occurs on the second version, which corresponds to the flight one.

In addition, we observed that the HF preamps systematically - and almost instantly - return to normal consumption after the pulses transients (those caused by the rising edge of the BIAS sweep). This excludes the latch-up hypothesis.

Finally, when the short circuit disappeared and the ANT#3 recovers its function, the observables revealed no difference in behavior before and after the anomaly.

About possible damages

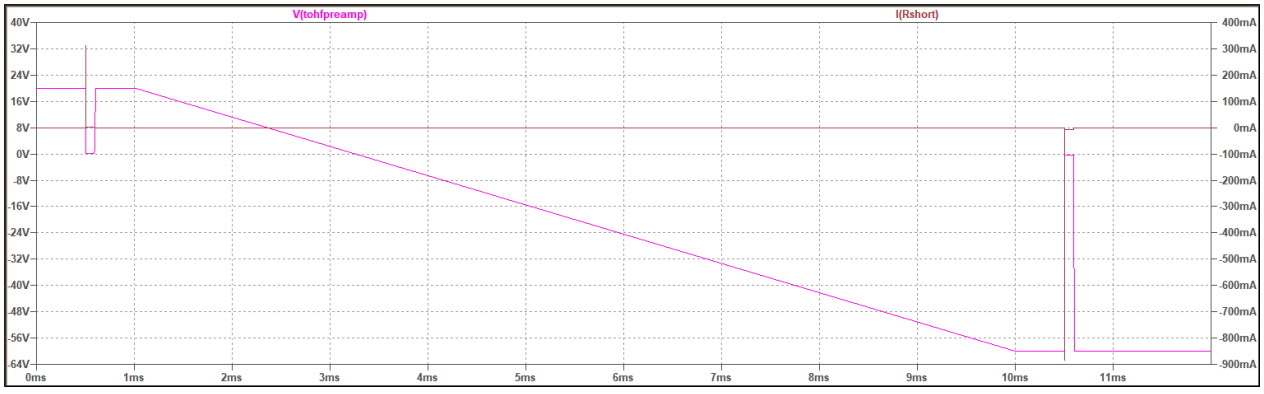
An analysis of a failure in the HF preamps and its propagation to the rest of the system easily shows that:

- Except PCB failure, a single fault in the HF PA (component breakdown) cannot propagate to the LF section and would not affect the LF operations. However, such failure would be visible on the data from the HF section.
- A double fault can propagate to the LF section, but this is very unlikely. In that case, it would have been clearly visible in the scientific and monitoring data.

In others words, if a preamp failure had occurred, its consequences would have been visible in scientific and monitoring data after the recovery of ANT#3 function. The observables did not reveal any obvious difference.

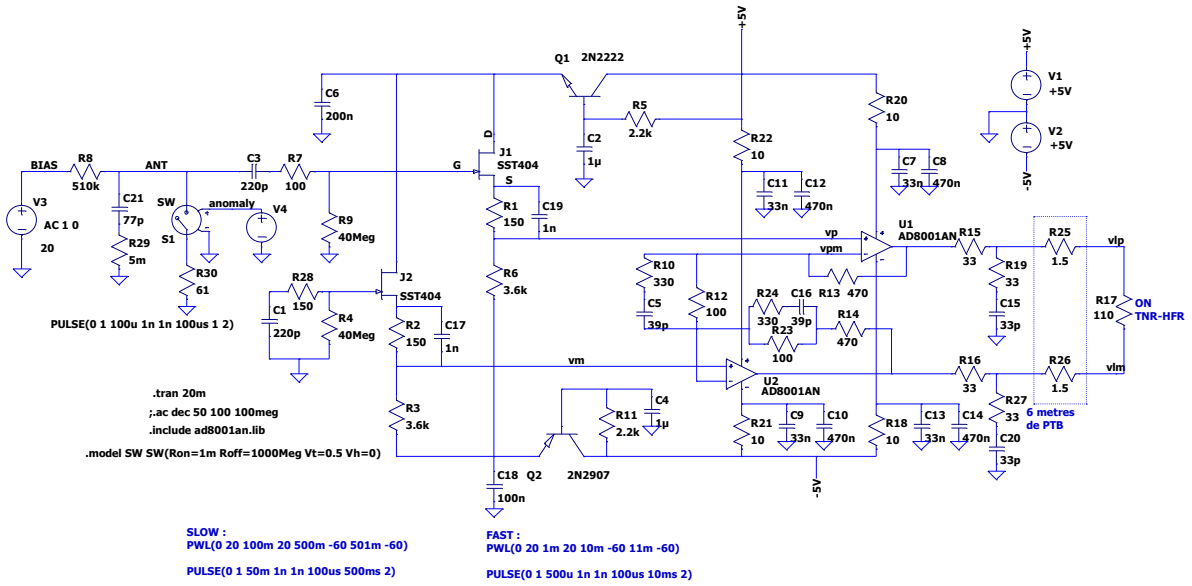
Part 2: Behavior of HF preamps when the fault appears

It is now a matter of reproducing as faithfully as possible the case of failure encountered on ANT#3. To do this, we propose to study the impact of the breakdown on the preamps by considering a ramp going from + 20V to – 60V (smaller than the previous one but closer to reality). Then, we superimpose a short circuit at the start of this ramp and at its end, as depicted below:



Simulation setup

The simulation configuration proposed here is similar to the previous one, but a circuit has been added to produce a sudden short circuit (under 61 ohms) at the preamp input... or at the base of the antenna as suspected.



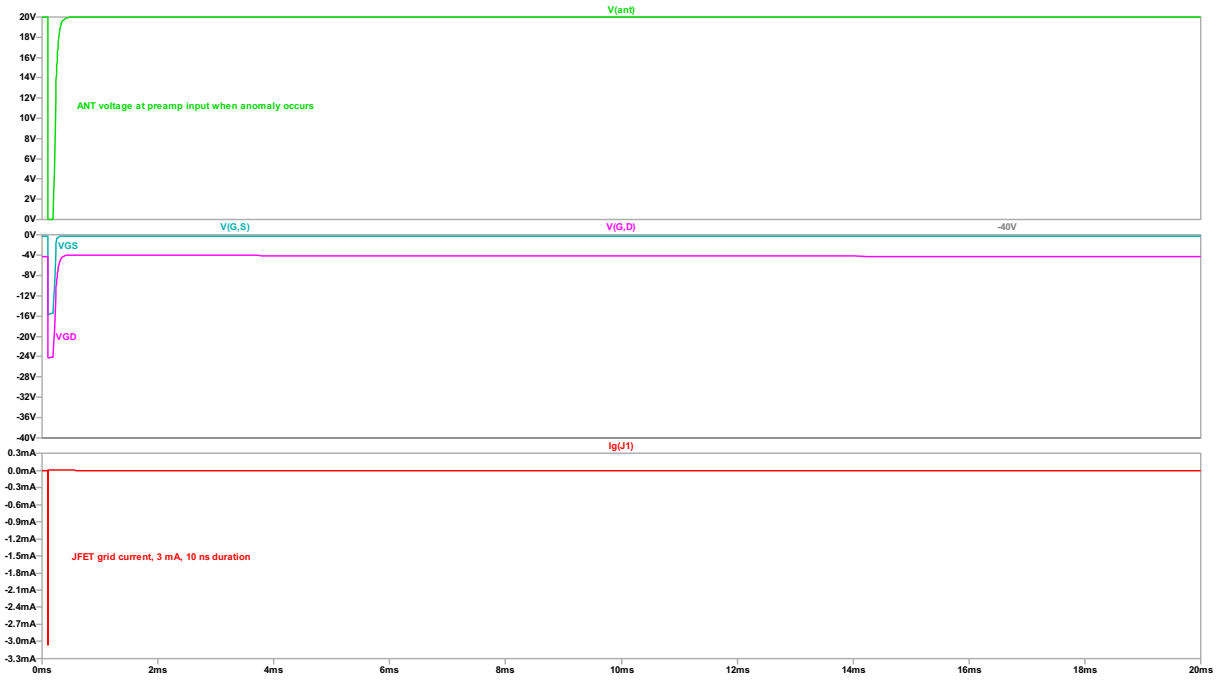
For the convenience of simulations, the BIAS weep ramp is not taken into account: it would unnecessarily increase the simulation duration without providing any significant benefit in the analysis (additionally, it prevents zooming in on short circuit events). We therefore removed it to focus the simulations on the two following cases:

- Transient from +20Vdc to ~0V, which supposes that the short occurs at the beginning of the ramp
- Transient from -60Vdc to ~0V, which corresponds to a short at the end of the ramp

In addition to the VGS and VGD (Grid to Source and Grid to Drain voltages), the plots below also show the current in the grid of the JFET stage; because this parameter is very impacted by the short circuit.

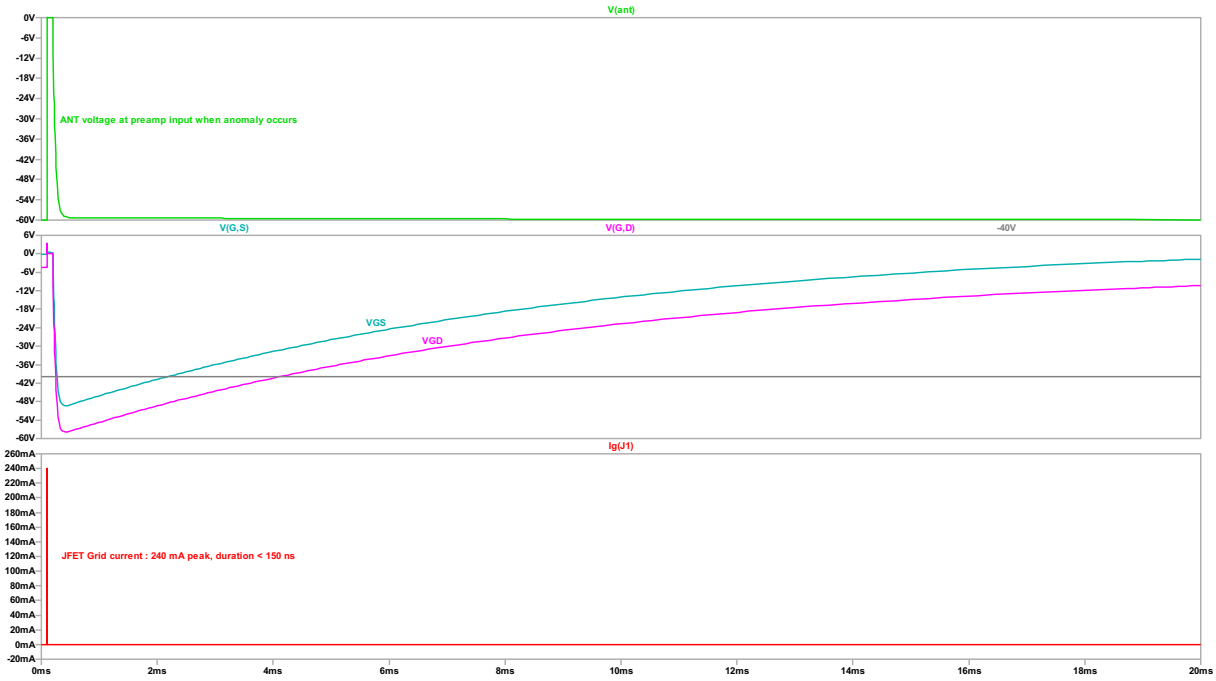
Simulation results

The first case (short circuit occurs when Vbias = +20Vdc) does not cause a problem, the derating on the JFET is respected and the peak current on its gate is below the authorized limit of 10mA.



The second case (short circuit when Vbias = -60Vdc) is more problematic:

- A significant current peak actually occurs on the JFET gate when the short circuit appears (rising transition from -60V to 0V). The peak is of 240 mA while the datasheet indicates a limit of 10mA. However, this only lasts about 100 ns.
- The derating limits on VGS and VGD (-40V) are exceeded for a few ms when the short circuit disappears (falling transition from 0V to -60V)



These two combined effects certainly constitute a stress for the JFET but fortunately, they are not destructive. This is especially because the charge contains in the current pulse is very low (Q ~ 240mA.100ns = **24nC**).